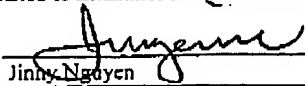


CERTIFICATE OF FACSIMILE

I hereby certify that this correspondence is being faxed to Examiner John J. Tabone, Jr. (703-872-9306) at the USPTO, on August 19, 2005.

  
Jinhy NguyenIN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Date: August 19, 2005

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Robert T. BAILIS et al.

Confirmation No: 5286

AUG 19 2005

Serial No: 10/016,449

Group Art Unit: 2133

Filed: December 10, 2001

Examiner: John J. Tabone, Jr.

Title: METHOD AND SYSTEM FOR USE OF A FIELD PROGRAMMABLE GATE  
ARRAY (FPGA) FUNCTION WITHIN AN APPLICATION SPECIFIC  
INTEGRATED CIRCUIT (ASIC) TO ENABLE CREATION OF A DEBUGGER  
CLIENT WITHIN THE ASIC

Mail Stop RCE  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Prior to examination, please amend the application as indicated on the following pages:

**Amendments to the Specification** begin on page 2 of this paper.

**Amendments to the Claims** are reflected in the listing of claims which begins on page 3  
of this paper.

**Remarks** begin on page 7 of this paper.